delay locking a plurality of clock signals to the reference clock signal so that the plurality of clock signals have respective phases relative to the phase of the reference clock signal.

58. (New) The method of claim 57 wherein the reference clock signal is locked to the same phase as the master clock signal.

59. (New) The method of claim 58 wherein a first of the plurality of clock signals has the same phase as the master clock signal, a second of the plurality of clock signals has a phase opposite the phase of the reference clock signals, and the remainder of the plurality of clock signals have respective phases that are spaced from each other between the phases of the first and second clock signals.

60. (New) The method of claim 59 wherein the remainder of the plurality of clock signals are spaced from each other between the phases of the first and second clock signals equally.

61. (New) A method of generating a sequence of clock signals from a master clock signal, comprising:

generating the sequence of clock signals each of which has a respective phase that increases from a first clock signal to a last clock signal in the sequence;

delay locking the first clock signal and last clock signals to each other so that they have a predetermined phase with respect to each other;

delay locking one of the clock signals to the master clock signal so that each of the clock signals in the sequence have respective phases with respect to the master clock signal.

62. (New) The method of claim 61 wherein the step of delay locking the first clock signal and the last clock signal comprises delay locking the first clock signal and the last clock signal so that they have respective phases that are 180 degrees from each other.

63. (New) The method of claim 61 wherein the step of delay locking one of the clock signals to the master clock signal comprises delay locking the first clock signals to the master clock signal.

64. (New) The method of claim 63 wherein the step of delay locking the first clock signal to the master clock signal comprises delay locking the first clock signal to the master clock signal so that they have substantially the same phase.

65. (New) The method of claim 61 wherein the step of generating the sequence of clock signals comprises generating the sequence of clock signals so that they have respective phases relative to the phase of the master clock that increase uniformly from a first clock signal to a last clock signal in the sequence.

66. (New) A method of generating a sequence of clock signals, comprising:

generating the sequence of clock signals which are increasingly delayed from a first clock signal to a last clock signal, two of the clock signals in the sequence being delay locked to each other so that they have a predetermined phase with respect to each other; and

delay locking one of the clock signals to a master clock signal so that the clock signals in the sequence have respective phases with respect to the master clock signal.

67. (New) The method of claim 66 wherein generating the sequence of clock signals comprises delay locking the first clock signal and the last clock signal to each other so that the first clock signal and the last clock signal have a predetermined phase with respect to each other.

68. (New) The method of claim 67 wherein the first clock signal and the last clock signal are delay locked to each other so that they are the inverse of each other.

69. (New) The method of claim 66 wherein generating the sequence of clock signals comprises increasingly delaying the clock signals in the sequence in equal increments

from the first clock signal to the last clock signal so that adjacent clock signals in the sequence have respective phases that are equally spaced from each other.

70. (New) The method of claim 66 wherein generating the sequence of clock signals comprises delay locking the first clock signal and the last clock signal so that they are the inverse of each other whereby the first and last clock signals have respective phases that are 180 degrees from each other.

71. (New) The method of claim 66 wherein delay locking one of the clock signals to a master clock signal comprises delay locking the first clock signals to the master clock signal so that they have substantially the same phase.

72. (New) The method of claim 66, further comprising selecting one of the clock signals to couple the selected clock signal to a clock output terminal.

73. (New) The method of claim 66 wherein the generating the sequence of clock signals comprises:

receiving a reference clock signal;

generating the sequence of clock signals from the reference clock signal by delaying the reference clock signal by respective delays that are a function of a control signal; and

comparing the phase of two of the clock signals in the sequence and generating the control signal as a function of the difference therebetween;

74. (New) The method of claim 73 wherein generating the sequence of clock signals comprises:

generating a first signal during the period that the phase of the first clock signal lags the phase of the last clock signal;

generating a second signal during the period that the phase of the first clock signal leads the phase of the last clock signal; and

generating as the control signal a voltage that increases toward one polarity responsive to the first signal and toward the opposite polarity responsive to the second signal.

75. (New) The method of claim 66 wherein delay locking one of the clock signals to a master clock signal comprises:

receiving the master clock signal;

generating a reference clock signal having a delay relative to the master clock signal that is a function of a control signal; and

comparing the phase of the master clock signal to the phase of one of the clock signals in the sequence and generating the control signal as a function of the difference therebetween.

76. (New) The method of claim 66 wherein the generating the reference clock signal comprises:

generating a first signal during the period that the phase of the master clock signal lags the phase of the one of the clock signals in the sequence;

generating a second signal during the period that the phase of the master clock signal leads the phase of the one of the clock signals in the sequence; and

generating as the control signal a voltage that increases toward one polarity responsive to the first signal and toward the opposite polarity responsive to the second signal.

77. (New) A method for providing a plurality of clock signals that have predetermined phases relative to a master clock signal, the method comprising:

producing a reference clock signal having a phase relative to the master clock signal that is a function of a first control signal;

generating the first control signal as a function of the difference in phase between the master clock signal and the reference clock signal;

producing the plurality of clock signals having respective phases relative to the reference clock signal that are a function of a second control signal; and

generating the second control signal as a function of the difference in phase between the reference clock signal and one of the plurality of clock signals.

78. (New) The method of claim 77 wherein the first and second locked loops comprise delay locked loops in which the first signal generator comprises a first voltage controlled delay circuit in which the master clock signal is delayed by a period determined by the first control signal to produce the reference clock signal, and the second signal generator comprises a second voltage controlled delay circuit in which the reference clock signal is delayed by a plurality of periods determined by the second control signal to produce the plurality of clock signals.

79. (New) The method of claim 77 wherein the reference clock signal having a phase relative to the master clock signal is one of the plurality of clock signals produced.

80. (New) The method of claim 77 wherein producing the first control signal comprises:

generating an enable signal during the period that the phase of the master clock signal lags the phase of the reference signal; and

generating as the first control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal.

81. (New) The method of claim 77 wherein producing the second control signal comprises:

generating an enable signal during the period that the phase of the reference clock signal lags the phase of the one of the plurality of clock signals; and

generating as the second control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal.

82. (New) The method of claim 77 wherein producing the plurality of clock signals comprises producing N clock signals, the phase of each of the clock signals relative to the phase of the master clock signal is [M/N]*180 degrees, where M=0, 1, . . N.

83. (New) The method of claim 77, further comprising selecting one of the plurality of clock signals to couple the selected clock signal to a clock output terminal.

84. (New) A method for providing a sequence of clock signals that have predetermined phases relative to a master clock signal, the method comprising:

generating a reference clock signal having a delay relative to the master clock signal that is a function of a first control signal;

generating the sequence of clock signals each of which has a delay relative to an adjacent clock signal in the sequence that is a function of a second control signal;

comparing the phase of the master clock signal to the phase of a first one of the plurality of clock signals and generating the first control signal as a function of the difference therebetween;

delay locking the phase of the first clock signal to the phase of the master clock signal;

comparing the phase of two of the plurality of clock signals and generating the second control signal as a function of the difference therebetween; and

delay locking the phases of the two clock signals to each other.

85. (New) The method of claim 84 wherein comparing the phase of two of the plurality of clock signals comprises comparing the phase of the first clock signal to the phase of a last clock signal in the sequence of clock signals.

86. (New) The method of claim 85 wherein delay locking the phases of the two clock signals comprises delay locking the first clock signal to the inverse of the last clock signal.

87. (New) The method of claim 85 wherein the clock signals in the sequence between the first and last clock signal are equally phased apart from each other and the first and last clock signals.

88. (New) The clock generator circuit of claim 84 wherein generating the first control signal comprises:

generating an enable signal during the period that the phase of the master clock signal lags the phase of the first one of the plurality of clock signals; and

generating as the respective first control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal.

89. (New) The clock generator circuit of claim 84 wherein generating the second control signal comprises:

generating an enable signal during the period that the first of the two clock signals lags the phase of the second of the two clock signals; and

generating as the second control signal a voltage that increases toward one polarity responsive to the enable signal and toward the opposite polarity responsive to the absence of the enable signal.

90. (New) The method of claim 84, further comprising selecting one of the clock signals to couple the selected clock signal to a clock output terminal.--

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REMARKS

Claims 57-90 are pending in the present application. Claim 1 has been cancelled and claims 57-90 have been added by amendment. Claims 57-90 have been added to claim embodiments of the invention described in the specification. No new matter has been added by new claims 57-90.